Design and Analysis of CMOS Frequency to Voltage Converter using 0.35µm technology

Kopal Gupta, Monika Bhardwaj, Prof. B. P .Singh

Abstract—This paper presents a 0.35µm CMOS frequency to voltage converter for portable applications which is based on a operating principle comprises a differentiator, voltage to current converter, two RMS-DC converters, and a divider. Results show that the converter has a power consumption of 11.89mW operating at 3.3V supply voltage. This converter can accurately convert a sinusoidal signal frequency into an output voltage with no ripples. Moreover, its output response has input amplitude independent characteristic. The simulation results are in good accordance with the theoretical analyses.

Index Terms— Current mode Circuits, Differentiator, Divider, Frequency-to-Voltage Converter, RMS-DC Converter, Translinear principle, Tanner EDA ,Voltage to Current Converter.

1 Introduction

Frequency to voltage or current converter is a device that generates an output voltage or current proportional to the frequency of a sinusoidal input signal. It has many applications in power control, communication, instrumentation and measurement systems, etc. The most known techniques used for frequency to voltage or current conversion are generally based on low-pass filtering of fixed duration at a rate set by the input frequency or counting the number of narrow pulses over a fixed period time [1-7]. Even though these techniques are widely used, they are based on complex circuits. Moreover, some of those have to use one or more reference signals with a very much higher frequency than the input signal. They are proposed by taking advantage of the mathematical characteristic of sinusoidal signals [8-9]. The frequency to voltage converter in [8] is realized by a differentiator, an integrator, a divider and a square-rooter. However, the division of the differentiator output to the integrator output causes large spikes when an initial value of the integrator is not zero. Unfortunately, an initial value of the integrator affects the converted output. Thus uncertain integral initial value makes the output of this technique inaccurate. In this paper, the frequency to voltage converter is presented which employs no additional integrators comparing to the previous converter.

So the integral initial value which influences the converted output as in [9] will not occur in the proposed converter. In other words, this technique provides much better accuracy than the previous technique. The simulations are conducted to confirm this idea and to illustrate the performances of the frequency to voltage converter. This paper is organized in six sections. Section 2 reviews the basic principle, circuit description and the implementation of Frequency to Voltage Converter. Simulation and Analysis of frequency to voltage converter is presented in Section 3 and finally the conclusions are reported in Section 4.

2 Frequency to Voltage Converter

2.1 Basic Principle

A frequency to voltage converter (FVC) is presented. It is composed of a differentiator, two RMS-DC converters, a divider and voltage to current converter. The block diagram is shown in Fig.1. Assuming that the input signal is a pure sinusoidal signal with a peak amplitude of A and input frequency of ω_{in},

$$v_{in}(t) = A\sin(\omega_{in}t) \quad (1)$$

Then, the derivative of this signal at the output of the differentiator can be written as

$$v_d(t) = A\omega_{in}\tau_d\cos(\omega_{in}t) \quad (2)$$

where τ_d is the time constant of the differentiator.

Feeding $v_{in}(t)$ and $v_d(t)$ into the voltage to current converter and then to RMS-DC converters yields the results as

$$I_{RMS1} = \frac{A}{\sqrt{2}} \quad (3)$$

$$I_{RMS2} = \frac{A\tau_d\omega_{in}}{\sqrt{2}} \quad (4)$$

respectively.

Thus dividing I_{RMS2} in (4) by I_{RMS1} in (3) yields

$$V_{out} = k\omega_{in} \quad (5)$$

where k is the sensitivity of the converter. It is clearly seen from (5) that the output signal is linearly proportional to the input frequency, ω_{in}, and insensitive to the input signal amplitude, A.

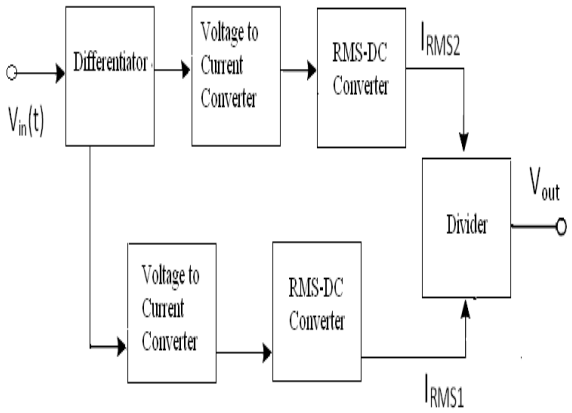


Fig. 1 Basic principle of the frequency to voltage converter

2.2 Circuit Implementation

2.2.1 Differentiator

The differentiator is sometimes called the rate of change circuit. In differentiator, the capacitor is in series with the signal line while the resistor is in parallel with the line. In this, the RC time constant is short compared with the period of the signal [10]. The operational amplifier makes it relatively easy to build high quality active differentiator circuits. Previously, one had to construct a stable, drift free, high gain transistor amplifier for this purpose. Again, the RC elements are used, but in a slightly different manner. The capacitor is in series with the op-amp inverting input, while the resistor is in the op-amp feedback resistor.

By introducing electrical reactance into the feedback loops of op-amp amplifier circuits, we can cause the output to respond to changes in the input voltage over time. Differentiator produces a voltage output proportional to the input voltage's rate of change. Capacitance can be defined as the measure of a capacitor's opposition to changes in voltage.The greater the capacitance, the more the opposition. Capacitors oppose voltage change by creating current in the circuit: that is, they either charge or discharge in response to a change in applied voltage. So, the more capacitance a capacitor has, the greater its charge or discharge current will be for any given rate of voltage change across it.

Figure3 shows the two stage op-amp based differentiator which measures change in voltage by measuring current through a capacitor, and outputs a voltage proportional to that current.

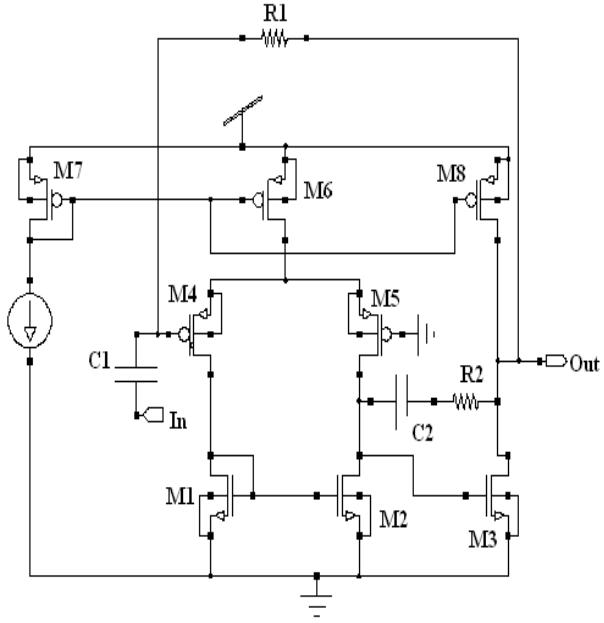
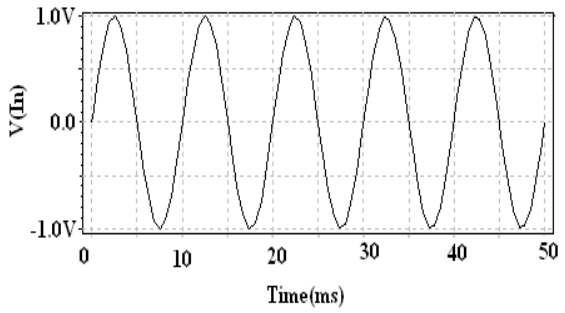
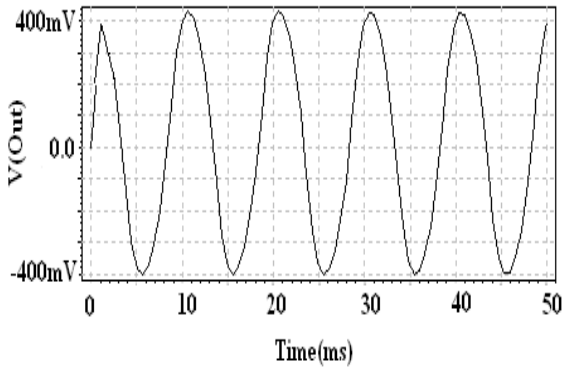


Fig. 2 Circuit diagram of differentiator

If the sinewave is applied to the input of differentiator then the result is the sinewave output that is shifted in –phase 90°.The circuit was simulated using T-Spice with 0.35µm TSMC CMOS process parameters. V_{dd}=3.3V, C1=60nF and R1=1k were employed. Fig. 3 (a) shows the time response of the differentiator for a sinusoidal input voltage with 1V peak amplitude and 100Hz frequency. Output of differentiator is cosine wave having peak amplitude of 400mV in Fig.3 (b).



(a) Input Voltage



(b) Output Voltage

Fig. 3 Time response of differentiator

The supply voltage is varied from 1.2 to 3.3V and then power consumed at different values of supply voltage can be obtained. Table1 shows values of power consumed for different values of supply voltages.

TABLE1
Power consumption with different supply voltage(V_{DD})

V_{DD} (volts)	Power consumption (in watts)
1.2	1.473143e-005
1.8	5.252552e-005
2.0	6.490663e-005
2.2	7.891860e-005
2.8	1.319304e-004
3.0	1.536498e-004
3.3	1.904340e-004

The variation of supply voltage of frequency to voltage converter is represented graphically in Fig. 4.

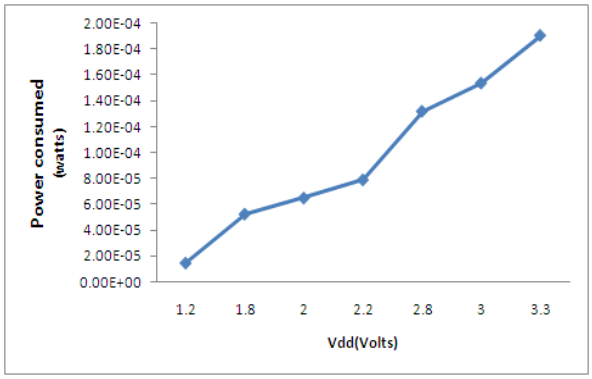


Fig. 4 Supply Voltage vs. Power Consumed Plot

2.2.2 RMS-DC CONVERTER

MOS translinear circuits can be categorized as follows [11]: stacked loop, up-down loop and electronically simulated loop. The stacked loop [12] similar to class-AB transconductance [13] suffers from body effect. Influence of the body effect in updown loop is smaller than in stacked loop but more circuits for current injection in transistors are required [14]. In Conventional circuit, a floating node in a circuit represents an error due to the fact that the initial condition is unknown unless it is somehow fixed. This generates two problems: first, it is not straight forward to simulate these circuits; and second, an unknown amount of charge might stay trapped at the floating gate during the fabrication process which will result in an unknown initial condition for the FG voltage as well as high power consumption and high cost. An RMS-to-DC Converter using electronically simulated translinear loop employing MOSFETs that are operating in saturation region is shown in Fig. 5. The circuit consists of three MOS transistors (M1, M2, and M3) and two op-amps. These two op-amps are employed for voltage mean operation and they force the gate voltage of transistor M3 to remain the mean voltage of the gate voltage of

transistors M1and M2. In other word, it can be written in mathematical form as follows:

$$V_{g3} = \frac{1}{2}(V_{g1} + V_{g2}) \qquad (6)$$

where V_{g1}, V_{g2} and V_{g3} are gate voltage of transistors M1, M2 and M3, respectively.

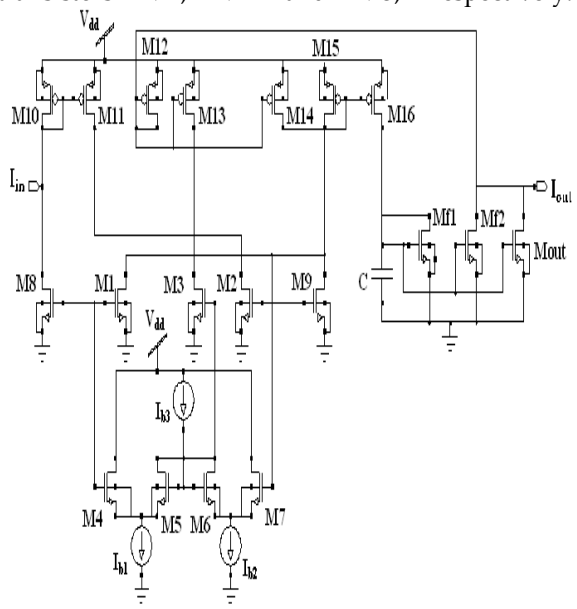


Fig. 5 Circuit diagram of the true rms-dc converter

Fig. 5 shows the circuit realization of the voltage mean operation, using transistors M4-M7 and current sources I_{b1}-I_{b3}.Employing the I-V relationships for transistors M1, M2 and M3 and the relations between current injections in translinear circuit and input/output currents of the squarer/divider are as the follows:

$$I_{in} = I_2 - I_1$$

$$\frac{I_{sq}}{2} = I_1 + I_2 - \frac{I_3}{2}$$

$$I_{out} = I_3$$

By changing the sign of I_{in} [15] the equation remains unchanged. This means that the input of the squarer/divider is two-quadrant and acts as a full wave rectifier. From Fig. 5, the sources of translinear MOS transistors are connected to the substrate, so the body effect is completely eliminated.

For a current-mode first-order low-pass filter, output current I_{outf} and input current I_{inf} in Laplace domain are related as:

$$\frac{I_{outf}(s)}{I_{inf}(s)} = \frac{1}{1 + \frac{s}{\omega_c}}$$

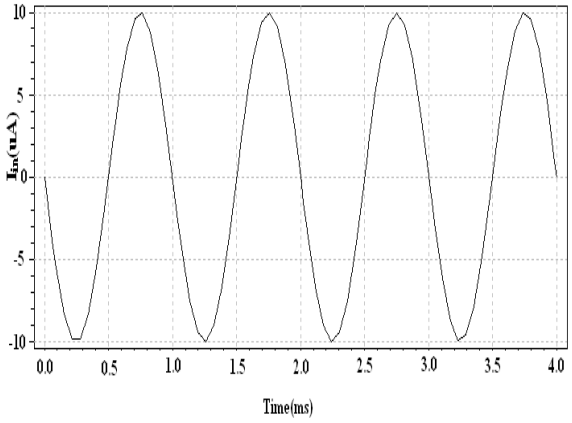
It can be shown that, for the input signal whose frequency is more than five times the cut-off frequency of the filter, output ripple will be less than 1% [16]. In such case, the output current of RMS-to-DC converter is a DC current I_{rms} with an ac ripple on it. The amplitude of this ripple is small compared to I_{rms}, i.e

$$I_{out} \cong I_{rms}$$

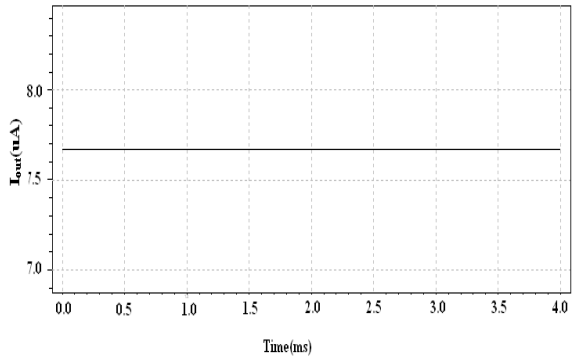
Considering these conditions it results that the values of the capacitor to achieve the accuracy of more than 1% is:

$$C \geq \frac{10\sqrt{KI_{rms,max}}}{\omega_{min}}$$

ω_{min} is the lower end of the frequency range and $I_{rms,max}$ is the output current higher end of the converter. The complete circuit diagram of the RMS-DC converter is depicted in Fig. 5. The circuit was simulated using T-Spice with 0.35µm TSMC CMOS process parameters. V_{dd}=3.3V, C=0.01pF and I_{b1}=I_{b2}=I_{b3}=1uA were employed. Fig. 6 shows the time response of the converter for a sinusoidal input current with 20µA peak-to-peak amplitude and 10 kHz frequency. The output is the dc current of 7.6µA which is same as rms value is shown in Fig. 6(b).



(a). Sinusoidal input current



(b). Output Current

Fig. 6 Time response of the rms-dc converter

The supply voltage is varied from 1.2 to 3.3V and then power consumed at different values of supply voltages can be obtained. Table2 shows values of power consumed for different values of supply voltages.

TABLE2
Power consumption with different supply voltage(V_{DD})

V_{DD} (volts)	Power consumption (in watts)
1.2	6.18E-06
1.8	9.28E-06
2.0	1.05E-05
2.2	1.30E-05
2.8	1.00E-04
3.0	1.62E-04
3.3	2.83E-04

The variation of supply voltage of frequency to voltage converter is represented graphically in Fig.7

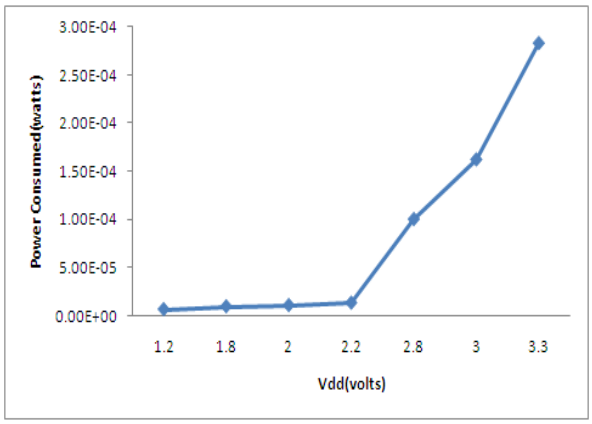


Fig. 7 Supply Voltage vs. Power Consumed Plot

2.2.3 VOLTAGE TO CURRENT CONVERTER

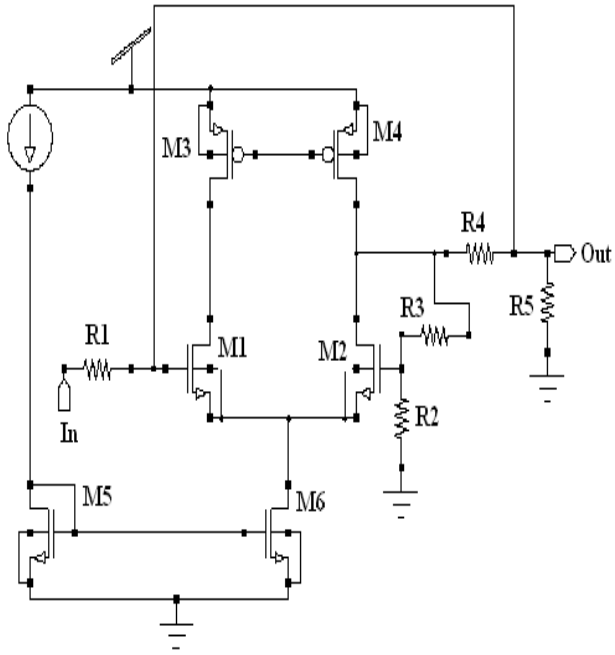
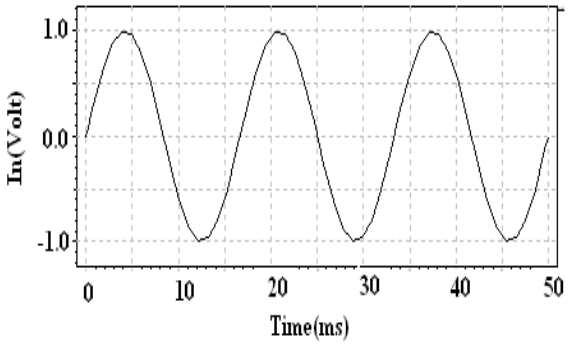
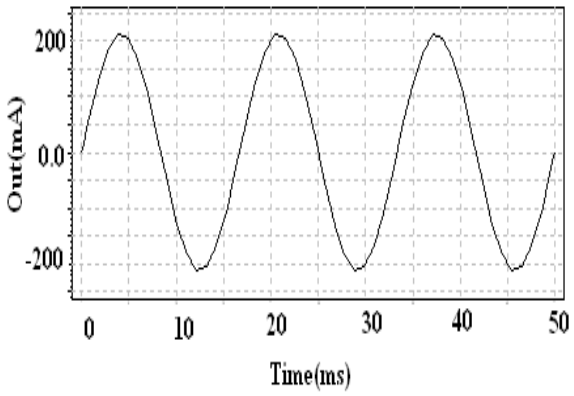


Fig. 8 Schematic of voltage to current converter

The circuit was simulated using T-Spice with 0.35µm TSMC CMOS process parameters. V_{dd}=3.3V, R1=R4=3.1ohm and R2=R3=R5=1ohm were employed.Fig.9 (a) shows the time response of the voltage to current converter for a sinusoidal input voltage with 1V peak amplitude and 100Hz frequency. Output of voltage to current converter is having peak amplitude of 200mA in Fig. 9 (b).



(a). Sinusoidal input voltage



(b). Output Current

Fig.9 Time response of voltage to current converter

2.2.4 DIVIDER

Analog dividers do mathematical operation of division of two signals (voltage or current). The idea is shown in Fig.10, where all transistors are working in current saturation mode. In this MOS resistor M3- M4, M6-M7 and M8-M9 form current mirror pairs. M5 and M10 are output stage transistors of MOS resistor. The output resistance seen through the terminal B into the grounded resistor (Input A grounded) is equal to R_{out}. Input current In2 is applied and output voltage gives divider function given by

$$v_{out}=In2*R$$

$$v_{out} = k\frac{In2}{In1}$$

Since the controlling current In1 has to be positive, this divider works only first-quadrant.

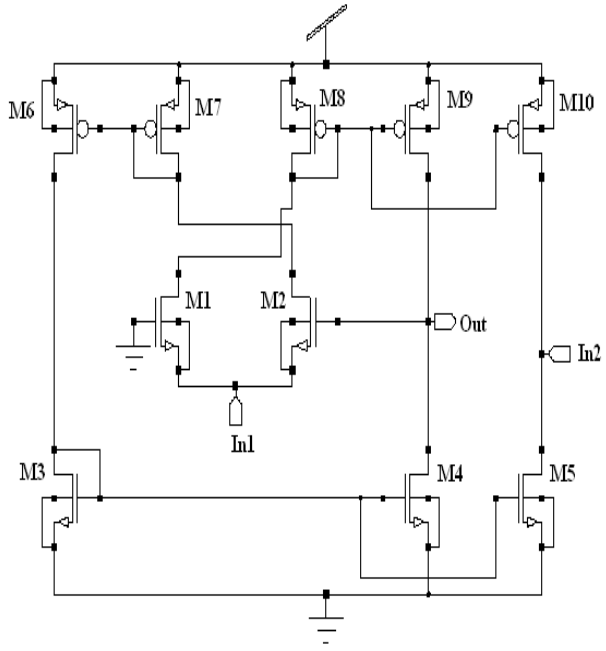
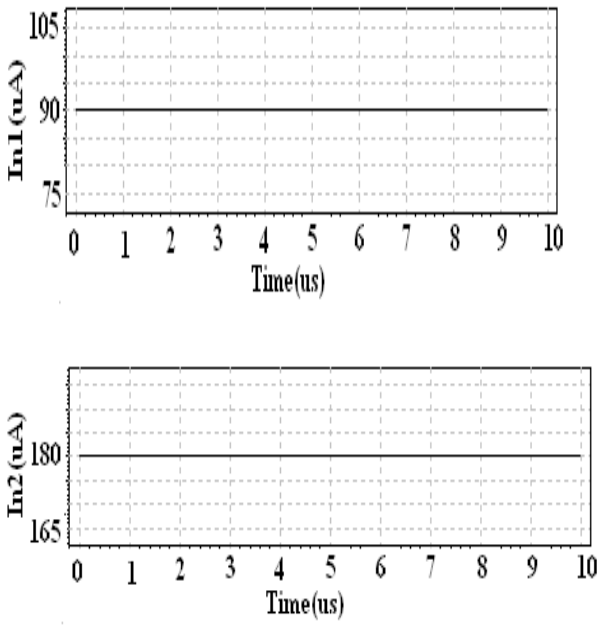
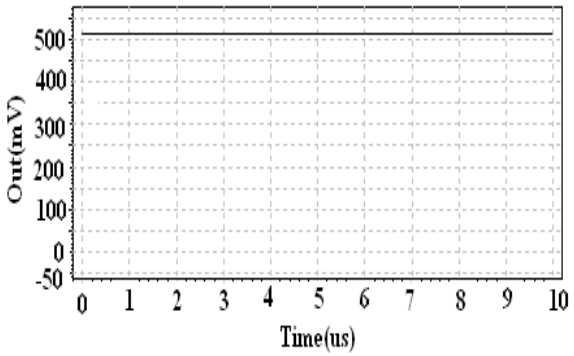


Fig. 10 Schematic of divider

The circuit was simulated using T-Spice with 0.35µm TSMC CMOS process parameters V_{dd}=3.3V were employed. Fig. 11(a) shows the input current In1 having dc value 90µA and In2 having 180µA.Fig. 11(b) shows the output voltage of 500mV.

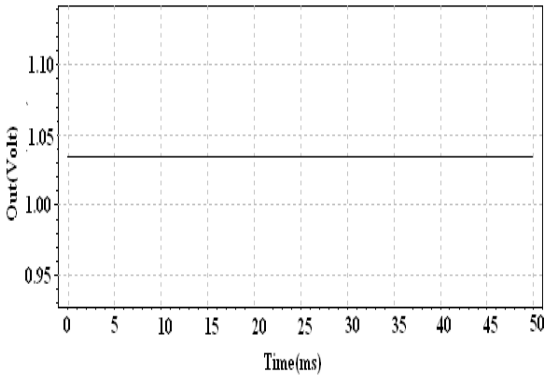


(a). Input Current In1 and In2



(b). Output Voltage

Fig. 11 Time response of the divider



(b). Output voltage

Fig.12 Time response of the frequency to voltage converter

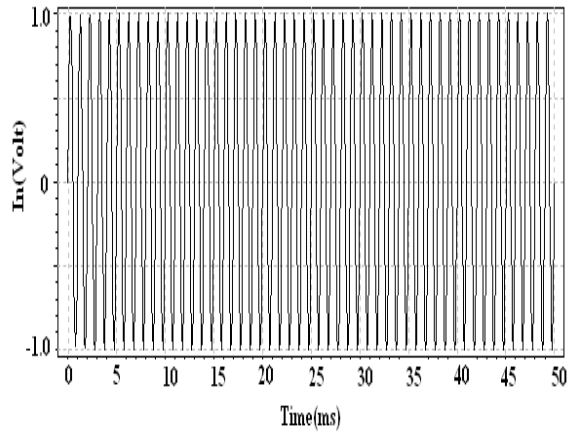
3 Simulations and Analysis

3.1 Simulation Environment

All the circuits have been simulated using 0.35µm technology on Tanner EDA tool.

3.2 Simulation Analysis

The complete circuit diagram of the frequency to voltage converter is depicted above in Fig.1. The circuit was simulated using T-Spice with 0.35µm TSMC CMOS process parameters with V_{dd}=3.3V. Fig.12 (a) shows a 1000 Hz sine wave signal with amplitude of 1 V which is applied at the input of frequency to voltage converter. Fig. 12(b) shows the dc output voltage of 1.04V without ripples.



(a). Input voltage

To demonstrate the input-amplitude independent characteristic, the sinusoidal signals at 1000 Hz with varying amplitude from 1 V to 5 V are applied to the FVC. It yields the result as shown in Fig. 13. It is obvious that the characteristic is significantly flat as expected.

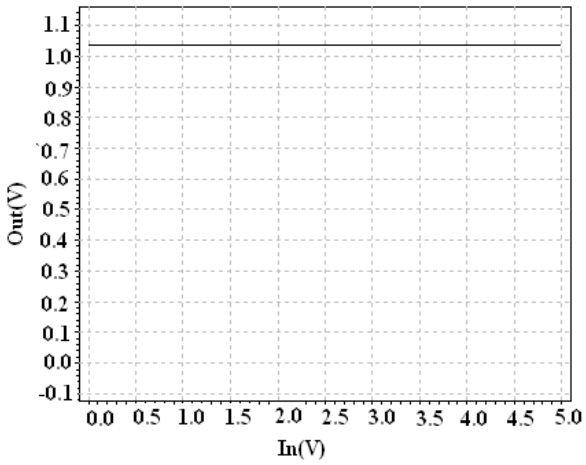


Fig. 13 Amplitude independent characteristics of frequency to voltage converter

The supply voltage is varied from 1.2 to 3.3V and then power consumed at different values of supply voltages can be obtained. Table3 shows values of power consumed for different values of supply voltages.

TABLE3
Power consumption with different supply voltage(V_{DD})

V_{DD} (volts)	Power consumption (in watts)
1.2	4.410055e-004
1.8	2.100061e-003
2.0	2.967266e-003
2.2	3.968086e-003
2.8	7.766710e-003
3.0	9.312802e-003
3.3	1.189842e-002

The variation of supply voltage of frequency to voltage converter is represented graphically in Fig. 14.

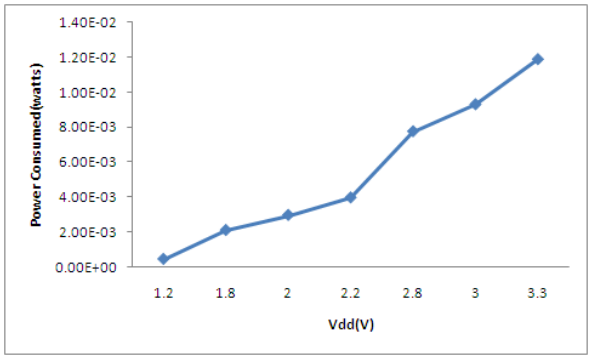


Fig.14 Supply Voltage vs. Power Consumed Plot

4 Conclusion

This paper has presented a technique of frequency to voltage converter. It is composed of a differentiator, voltage to current converter, two RMS-DC converters, and a divider. Since no additional integrators are exploited, it is superior to the conventional FVC because of no initial value effect. This FVC provides accurate measurements. The simulation results are in significant agreement with the theoretical. Moreover, the detected characteristic is independent of input amplitude.

Acknowledgment

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